



Product Acquisition Case Study

JPL Deep Space Network Telemetry Processor



RT Logic!

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Aggressive TLP Project Delivery Schedule

Month 1	Month 2	Month 3	Month 4	Month 5	Month 6	Month 7	Month 8	Month 9
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▲ Authorization to Proceed

▲ Software Simulator Chassis

▲ ————— Development/Integration ————— ▲

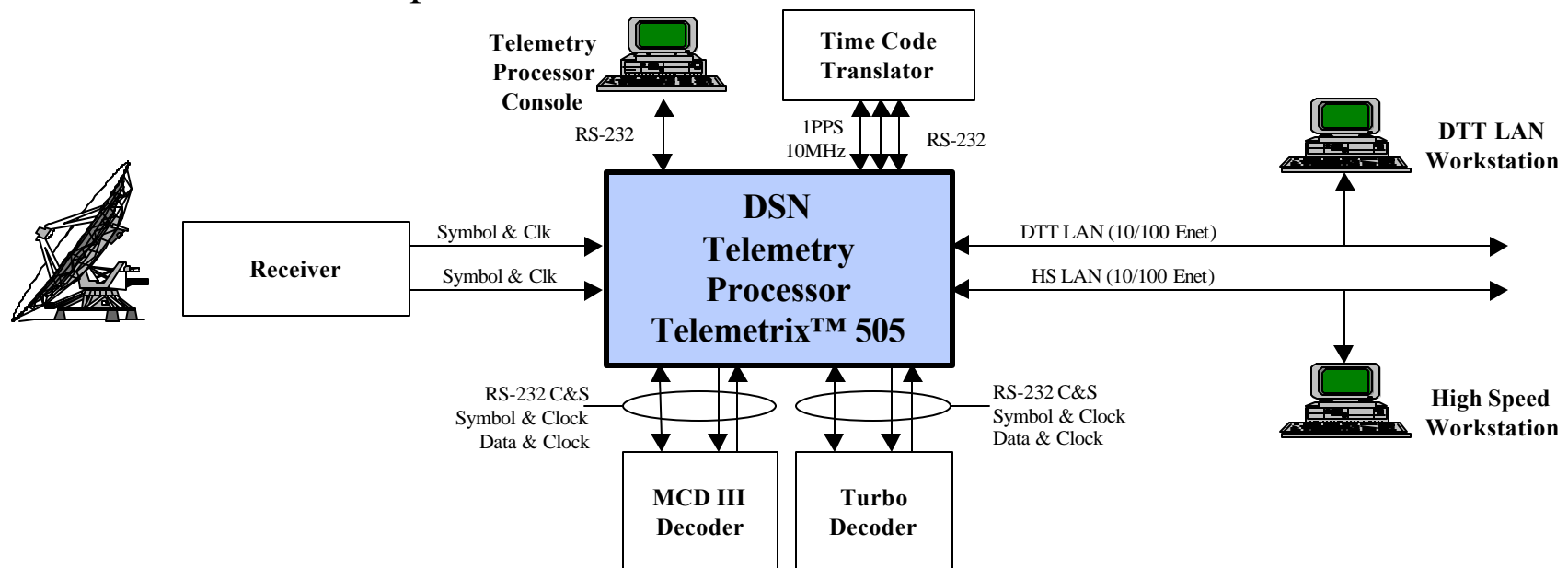
▲ ————— System Test ————— ▲

▲
TLP & Software

- Firm-Fixed-Price Contract
- Deliverables:
 - One TLP Software Simulator – 2 Months After Receipt of Order (ARO)
 - Three Fully Functional and Tested TLPs
 - System Software
 - Complete Documentation
 - Level-of-Effort Engineering
 - 5 Year Warranty
 - Production Systems

Ambitious TLP Technical Objectives

- Support Downlink Viterbi Decoding, Reed Solomon Decoding, and Frame Synchronization for JPL's Deep Space Missions From 2bps To 13.2 Symbols/Sec., 4-26.4 Mbps
- Capture Every Bit – Partial Frames, Uncorrected Data
- Support External MCD III & Turbo Decoder Interfaces
- Interface With JPL's Legacy Real Time Software For Data Processing
- Maximize Use of COTS Hardware and Software
- Provide an Open Architecture Platform With A View Towards System Extension/Expansion



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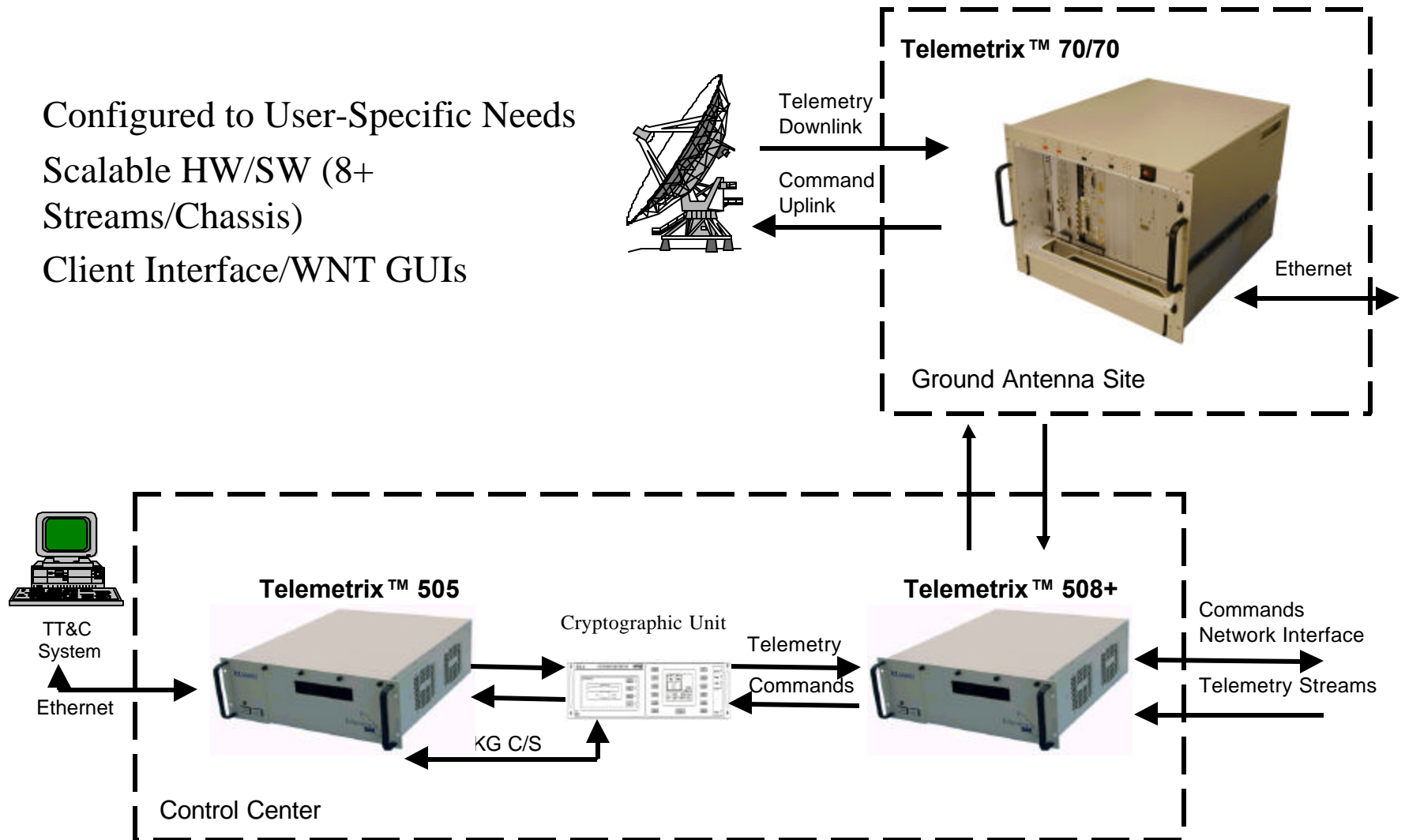
Telemetrix™ – It's THE Architecture!

TLP Solution Leverages COTS/Open Software

- RT Logic Telemetry™ 505 Hardware Platform
 - 12-Slot Modified COTS VME Chassis
 - Motorola PowerPC Master CPU
 - Radstone PowerPC CPU Hosts Legacy JPL Software
 - Avtec Systems 7001 Viterbi Decoder (New Development)
 - Avtec Systems 6130J PMC Reed Solomon Decoder (Modified COTS)
- RT Logic Telemetry™ Software Architecture Implementation
 - COTS VxWorks Real-Time Operating System
 - COTS RT Logic Device Drivers/API For Avtec Systems Hardware
 - COTS Clients and Servers for Control and Status
 - Driver Interface Used for Data Delivery
 - Simulators Provided For Each Device – Able to Run Without Final Hardware

Based on Existing Telemetry™ System Architecture

- Configured to User-Specific Needs
- Scalable HW/SW (8+ Streams/Chassis)
- Client Interface/WNT GUIs

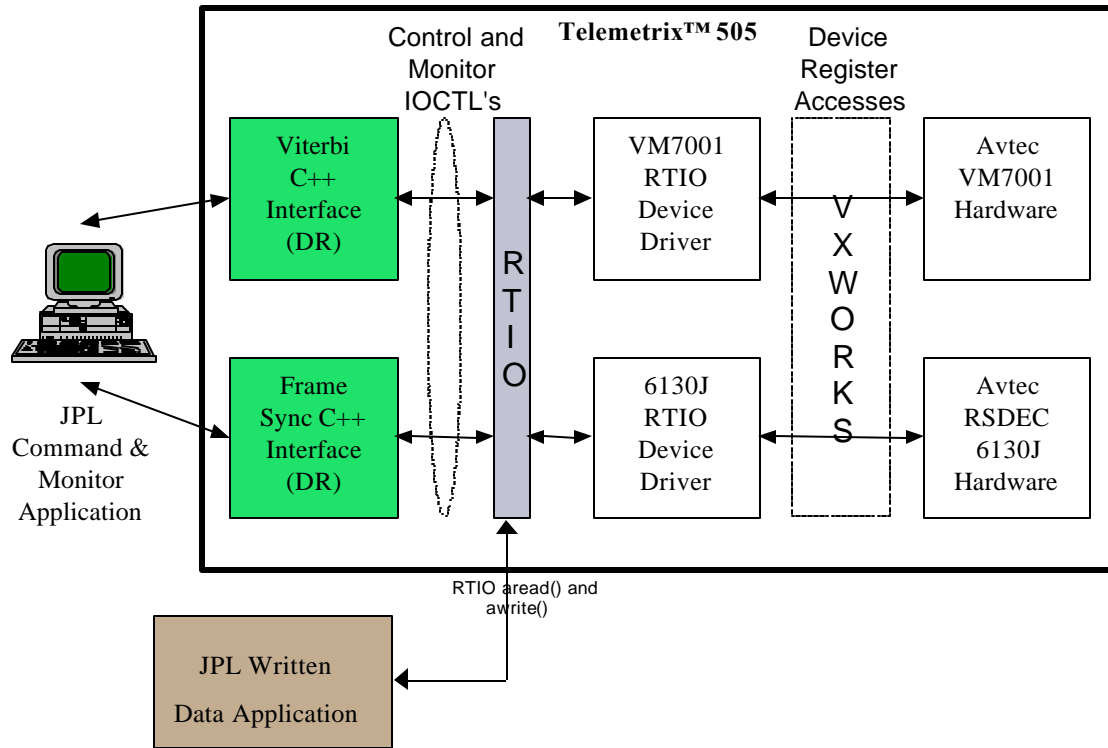


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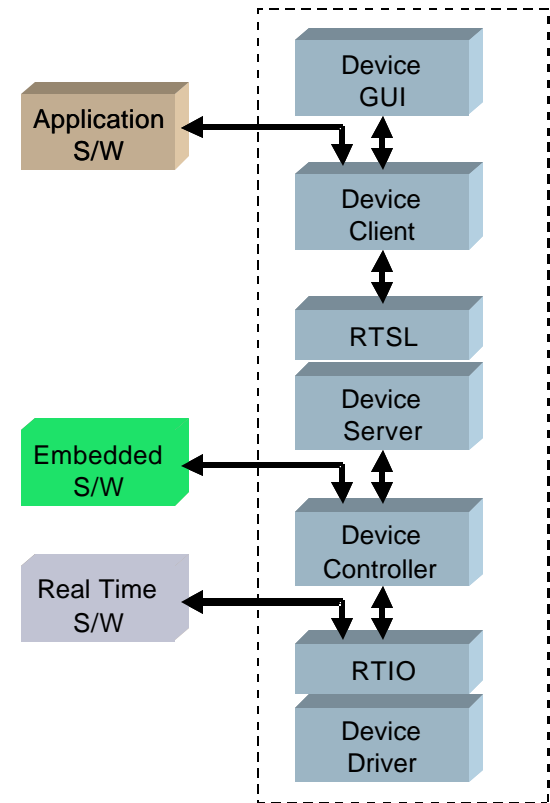
Telemetry™ – It's THE Architecture!

Open Software Architecture Promotes Integration

TLP Software Interface



RT Logic Telemetrix™ Software



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Telemetrix™ – It's THE Architecture!

Software Architecture is Modular and Layered

- Driver Layer Has A Common API To Higher Level Application Tasks (Open, Close, Read, Write, IOctl)
 - Utilizes Real Time I/O (RTIO) Library Product
 - All Drivers Have Identical API
- Device Wrapper Layer Encapsulates Hardware Device Specifics Within a Class
 - Provides Identical API As Client: Very Useful for Simulation
 - Allows Hardware Independence
 - Lowers System Life-cycle Cost – H/W Upgrades are Transparent to Application S/W
- Device Server Layer Utilizes Real Time Server Library (RTSL) to Implement Network Interface
- Device Clients Provide C++ Method Calls For Each Controllable Parameter
 - Utilize ACE Platform-Independent Libraries To Support Unix/Linux, Windows, VxWorks
 - C++ Interface to Most Customer Applications – Far Easier/More Reliable Than An ICD!
- GUIs For Windows

JPL Telemetry Processor Benefits

- Software Simulators for the ‘Front-End’ Hardware
 - Minimized System Integration Time – Facilitated JPL S/W Development
 - Reduced Software Engineering Support
- Device Wrapper Encapsulation of Device-Specific Attributes
 - Provides Hardware Vendor Independence
 - Lowers Life-cycle Costs
- Layers Allow Interfacing at Multiple Points – Driver, Real-Time Application, Network Application
- Open Architecture Minimizes Legacy Software & Hardware Interface Issues
- Use of COTS Hardware and Software
 - Leverages Large Investment Base
- Comprehensive Testing

Other Programs Have Benefited From The Telemetry Architecture

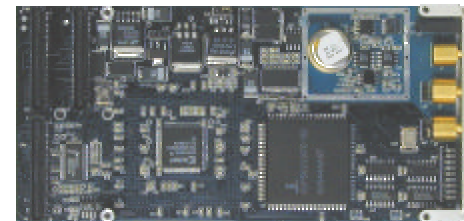
- GPS Station Computer System Replacement (SCSR)
 - Telemetry, Commanding, SGLS Ranging and AFSCN Interface Systems
 - Straightforward KG Migration (KIT-123/KGR-28A to KI-17)
 - Common Hardware and Software Interface
 - Interface To OS/COMET Ground Station Software
- SBIRS High Ground Sites and Mobile Terminals
 - Telemetry Acquisition, Commanding, KG Interface, AFSCN Interface Systems
 - Interface to SCS-21 Ground Station Software
- RCDC Quick Reaction Demonstrator (QRD)
 - Telemetry Acquisition, Commanding, SGLS Ranging
- DSCS Replacement Satellite Command and Control Element (RSCCE)
 - Telemetry, Commanding, KG Interface
 - Interface to Legacy VAX Software

The Next Step – Real Time Programmable Hardware

- Field Programmable Logic Allows One Hardware Module to Take On Multiple ‘Personalities’ Depending Upon The Mission
 - Firmware Can Be Downloaded At Run-Time or On The Fly – Much Like Software
 - VHDL – C++ For Firmware Developers
 - Firmware ‘Objects’ – Building Blocks for Firmware Personality
- Reduces O&M Training Costs
 - Multiple System Functions Provided By Common Hardware Device
- Reduces Sustainment Costs
 - Common/Fewer Spares
 - Firmware Upgrades to Support New Hardware Functions



- Front-End Function Processor (RTL-FFP)
 - Dual Frame Synchronizer
 - Dual PCM Simulator
 - Command Formatter
 - KG Controller
 - AFSCN Interface
 - IRIG Time Processing



- Baseband Digital Processor (RTL-KEYPMC)
 - PSK Demodulation
 - Bit Synchronization
 - Frame Synchronization
 - FM Discrimination
 - SGLS Demodulation

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Telemetry™ – It's THE Architecture!

Summary

- JPL TLP Project was Successful COTS-Based Development
- Open, Layered, Modular Software Architecture Maximized COTS Software Reuse and Allowed Custom Real Time Software Development
- Open Hardware Architecture Supported Legacy Hardware
- Software Simulators Allowed Concurrent RT Logic and JPL Development
- Vendor/Customer Interfaces Communicated Openly
- TLP Implementation Supports Future Upgrade
- Delivered Within Cost/Schedule